REMARKS

These remarks are in response to the Office Action mailed on March 3, 2003. The Office Action rejected claims 15-17 under 35 U.S.C. 112, second paragraph, claims 1, 3-7, 10, 12, 18, 19, and 22 under 35 U.S.C. 102(b) as anticipated by Roberts et al. (U.S. patent number 5,576,757), and claims 2, 11, 13, 14, 16, 17, 20, 21, 23 under 35 U.S.C. 103(a) with Roberts et al. as the primary reference. (No specific reasons appear to be given for the rejection of claims 8 and 9.) The Office Action also objected to claims 13 and 17, along with the Figures and Specification. These are all discussed below under the appropriate heading.

Objections to Drawings and Specification

The Office Action Objected to the Drawings due to the lack of a number of reference signs. The Applicants thank the Examiner for noting these omissions, which have been rectified by the present Amendment. (The specification respectively cites reference signs 630, 725, and 735 at page 25, line 19, page 27, line 18, and page 27, line 26.) As the added text is a simple description of what the reference numbers refer to in the corresponding figures, this does not constitute the introduction of new matter.

The Office Action also objected to the disclosure due a missing application number on page 11, line 19. This number has now been supplied.

Objections to Claims

The Office Action objected to claim 13 due to a lack of clarity as a result of the indentation used, aggravated by the way the claim was divided between pages. The Examiner's interpretation of the claim appears correct and the indentation of the claim has been rationalized, thereby removing the basis of the objection. Additionally, the informality noted in claim 17 has been corrected.

Rejections under U.S.C. 112, second paragraph; New Claim 24

The Office Action rejected claims 15-17 under U.S.C. 112, second paragraph, due to insufficient antecedent bases in claims 15 and 16. These claims have now been amended to conform to the Office Action's remarks.

The Office Action has also indicated the allowability of claim 15, aside from the U.S.C. 112, second paragraph, rejection, for the reasons stated in the Office Action.

Consequently, claim 15 has additionally been represented in independent form and is therefore now believed allowable. New claim 24 is modeled on claim 15 and contains the same limitation of the present invention that the Office Action has indicated as allowable, but lacks some of the other, intervening limitations of claim 15. Therefore, claim 24 is similarly believed allowable.

<u>102/103 rejections and new claims 25 and 26</u>

The Office Action rejected claims 1, 3-7, 10, 12, 18, 19, and 22 under 35 U.S.C. 102(b) as anticipated by Roberts et al. (U.S. patent number 5,576,757), where claims 1 and 18 are respectively independent device and method claims. The Applicants respectively submit that these rejections are not well founded for a number of reasons.

Beginning with claim 1, this states

> A digital imaging system comprising:
> an image sensor;
> image processing and compression circuits; and
> a high density analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits.

The Office Action identifies the image sensor with CCD 1 (Figure 2) and the image processing and compression circuits with elements 10-12 (Figures 2 and 5A) of Roberts. The last element is identified with the sample and hold circuitry 18 of Figure 5A.

As described in Roberts (column 3, lines 14-16), "Figure 5A is a schematic block diagram showing the image signal to digital signal conversion logic", where the details of this figure are given starting column 7, line 7. The sample and hold elements are part of the analog to digital conversion circuits in Roberts and, although a portion of the data from the image sensor flows through them for sampling, they are not an analog/multi-level memory, either as these terms are commonly used or as they are used in the present application. Rather, as the name implies, a sample and hold circuit briefly holds some information derived from the input signal in a sampling process so that a digitization can take place---it is not the sort of high density analog/multi-level memory as recited in the claim, where the "high-density" has been added to further clarify this distinction.

Additionally, the Office Action's identification of the sample and hold element 18 of Roberts is inconsistent with the Office Action's rejection of claims 4 and 12, where the same

sample and hold element is (more correctly) placed as part of the "image processing and compression circuits". Although sample and hold circuits may be included in a memory, the are not in and of themselves a memory, such as the memory of the Simko reference cited with respect to claim 2: the device of Simko does contain sample and hold circuits, but these are peripheral circuits on the memory and not for storing the data.

Also, as the sample and hold elements 18 are part of the image processing and compression circuits (and are so identified in claims 4 and 12), they are not "between said image sensor and said image processing and compression circuits", but instead a part of the processing circuits.

Additionally, as the sample and hold circuits are part of the analog to digital conversion circuits, they do not "transmit said analog data", but rather take a sample of the analog data and supply a portion of the digitized version of this data.

Thus, the cited sample and hold elements are part of the image processing and compression circuits, they are not a memory---and, in particular, not a high density memory---and they do not transmit analog data, but rather convert analog data to digital data. This differs from the final element of claim 1:

> a *high density analog/multi-level memory* coupled *between* said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and *transmit said analog data* to said image processing and compression circuits.

As the added emphasis shows, this final element of claim 1 is between the image sensor and processing/compression circuits (not part of the processing/compression circuits), is a high density memory (as opposed to a peripheral element of very limited capacity), and transmits its contents in analog form (and not converted to digital form). For any of these reasons, it is believed that a rejection of claim1 under 35 U.S.C. 102(b) as anticipated by Roberts et al. is not well founded and that claim 1 and its dependent claims, claims 2-14, 16, and 17, are allowable.

(It should again be noted that, with respect to claims 4 and 12, the Office Action is inconsistent between the rejection of claim 1 (where the sample and hold element is taken as the memory) and the rejection of claims 4 and 12 (where it is taken as part of the image processing and compression circuits).)

Considering claim 18, it is believed allowable for reasons similar to those described above with respect to claim 1. Specifically, claim 18 states:

> A method for digital imaging, the method comprising:
> converting an image into electrical signals;
> storing said electrical signals as analog data; and
> transmitting portions of said analog data for digital signal processing.

As with claim 1, the last element again describes transmitting the *analog data* that was previously stored, rather than converting the analog data to digital form, as would be the case for the sample and hold circuitry of Roberts et al.. Although claim 18 states that this analog data is transmitted for digital processing, it is (contrary to the teachings of Roberts et al.) transmitted in analog form. Similarly, it is after the analog data is stored and transmitted (in analog form), that any digital processing takes place, whereas the sample and hold element of Roberts which the Office Action identifies as the storing element is rather part of the digital signal processing, namely, the analog to digital conversion.

As for the "storing said electrical signals as analog data" element of claim 18, as is clear from the preceding element, "said electrical signals" correspond to the "image": that is, it is the image that is stored, not just a portion of it. As discussed above, in Roberts et al., it is only a part of the image (the particular pixel or pixels currently being digitized) that is passing though the cited sample and hold elements of Roberts et al. at given time, as is believed clear from the patent's Figure 5A and its description. Referring to Figure 5A, a PIXEL MULTIPLEXER 7 is placed between the input from the CCD array and the S/H elements 18, so that "*each charge, when addressed*, is amplified and processed in a sample and hold (S/H) circuit 18" (column 7, lines 7-9, emphasis added). Consequently, the device of Roberts et al. lacks the process of "storing said electrical signals as analog data", where the "said electrical signals" are the image. (It should be noted that further down (col. 7, ln. 49, to col. 8, ln. 8), Roberts et al. describe the use of several such S/H arrangements in parallel, which would increase the storage somewhat, but these teaching still describe less than the whole image passing through at any given time. Additionally, it is believed that the given discussion further accentuates the distinction in function and structure between the sample and hold circuits of Roberts et al. and the high-density analog/digital memory of the present invention. In any case, the sample and hold circuits are again part of an analog to digital conversion and not a memory.)

The Office Action rejected claim 2 under 35 U.S.C. 103(a) with Roberts et al. as the primary reference and Simko (U.S. patent number 4,989,179) as a secondary reference. Although already believed allowable as it has claim 1 as its base claim, claim 2 is believed allowable for additional reasons.

It is admitted in the Office Action that claim 2 recites features which the Simko patent does not explicitly show. Yet there is no further reference or other evidence of prior art presented to demonstrate that the overall claimed combinations including the elements missing from Simko and Roberts et al. would have been obvious. The Office Action summarily states that "it would have been obvious" to add the missing elements to Simko and Roberts et al. in order to meet the terms of the claims. It is respectfully admitted that assumptions have improperly been made by the Examiner as to what one ordinarily skilled in the art would have found obvious to do since there is no supporting evidence provided in the Office Action. It is respectfully submitted that these rejections do not make the necessary *prima facie* case of obviousness, and that, on that basis, the rejection of claim 2 must be withdrawn.

More specifically, the Office Action states that it would have been obvious that "using enough columns would permit any amount of data to be stored for any length of time." While, in a limited sense, it may be true that adding more columns may increase memory capacity and that the Office Action is correct when it quotes Simko as stating that the "'actual number [of columns] is not preordained, but may be chosen by the practitioner depending on signal quality desired"(column 5, lines 42-44)", increasing capacity is not the same as increasing the speed of a memory. Merely adding more columns to the memory of Simko would not result in a memory that receives "data at a rate of greater than 10 Mbits/sec for more than 5 seconds and stores more than 50 Mbits of said data", as recited in claim 2. It is respectfully submitted that producing a memory of this performance is neither taught by nor obvious from the teachings of Simko and is rather more complex than just adding on additional columns.

Simko does mention using a sampling rate of 8 KHz (column 5, line 41, and column 6, lines 21 and 48, and elsewhere), but this is only a sampling rate related to the conversion of an analog signal to digital form. In any case, Simko does not disclose or suggest the sort of values for data rate (10Mbits/sec), duration (5 seconds) or capacity (50 Mbits). (At column 8, lines 12-23, Simko does describe recording up to one second of sound, not image, data, but

goes on to describe (column 8, 21-23) that even this amount of audio data would require 8 times the memory capacity of what is taught in this patent.

Consequently, it is respectfully submitted that the rejection of claim 2 under 35 U.S.C. 103(a) with Roberts et al. as the primary reference and Simko as a secondary reference is not well founded and that claim 2 and its dependent claims (13, 14, 16 and 17) are further believed allowable for any of these reasons.

Although indicated as rejected on the cover sheet, the Office Action gives no explicitly reasons for the rejection of claims 8 and 9. These claims are believed allowable as their underlying claims are believed allowable, as is described above. These claims are further believed allowable for the additional limitations of placing the memory and the A/D converter on a removable card, a limitation that is neither found in nor suggested by the prior art.

A number of the dependent claims are believed allowable for additional reasons that will not be discussed further at present in order to save space. For instance, with respect to claim 19, the Office Action states that "red, green, and blue signals are amplified before being stored in the sample-and-hold circuitry 18 (column 7, lines 7-9)." This is respectfully submitted to be incorrect: the cited location reads "each charge, when addressed, is amplified and processed *in* a sample and hold (S/H) circuit 18". As the added emphasis shows, the referred to amplification occurs *in* the sample and hold circuit (which, as argued above, is part of the image processing circuits *after* the memory), and is not pre-processing *before* the memory.

New claims 25 and 26 have been added. These are drawn to the aspect of the present invention whereby the analog data stored in the memory may be accessed in its analog form, as is shown, for example in Figure 2 of the present application where elements 230, 240, and 280 access the contents of memory 210.

Conclusion

For these reasons, claims 1-26 are believed allowable. Reconsideration of claims 1-23, and consideration of new claims 24-26, is respectfully requested and an early indication of their allowability is earnestly solicited.

Respectfully submitted,

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1.(Amended) A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

a high density analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits.

2. The system of Claim 1, wherein said memory receives said data at a rate of greater than 10 Mbits/sec for more than 5 seconds and stores more than 50 Mbits of said data.

3. The system of Claim 1, wherein said analog data comprises image data.

4. The system of Claim 1, wherein said image processing and compression circuits comprise an analog-to-digital (A/D) converter.

5. The system of Claim 4, wherein said image processing and compression circuits further comprise an image compressor.

6. The system of Claim 1, wherein said memory transmits portions of said data when said image processing and compression circuits are available for processing said data.

7. The system of Claim 5, wherein said image sensor, image processing and compression circuits, and memory comprise a digital still camera.

8. The system of Claim 7, wherein said memory is contained in a removable memory card.

9. The system of Claim 8, wherein said A/D converter is contained in said removable memory card.

10. The system of Claim 7, wherein said image processing and compression circuits are contained within the body of said digital still camera.

11. The system of Claim 7, wherein said image processing and compression circuits are not embedded within the body of said digital still camera.

12. The system of Claim 7, wherein said image sensor, image processing and compression circuits, and memory are contained within the body of said digital still camera.

13.(Altered indentation) The system of Claim 2, wherein said memory comprises:

a plurality of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell;

a timing circuit coupled to sequentially start programming operations by the write circuits; and

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming operations.

14. The system of Claim 13, wherein the memory is an analog memory.

15.(Amended) A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

an analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits, wherein said memory receives said data at a rate of greater than 10 Mbits/sec for

more than 5 seconds and stores more than 50 Mbits of said data and, wherein said memory comprises:

a plurality of write pipelines each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell;

a timing circuit coupled to sequentially start programming operations by the write circuits; and

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming operations, and

wherein the write pipelines comprise:

a plurality of odd numbered pipelines; and

a plurality of even numbered pipelines,

wherein when an odd numbered pipeline and an even numbered pipeline are both performing programming operations, a selection circuit in the odd numbered pipeline selects the first voltage when a selection circuit in the even numbered pipeline selects a second voltage and a selection circuit in the odd numbered pipeline selects the second voltage when the selection circuit in the even numbered pipeline selects the first voltage.

16.(Amended) The system of Claim 2, wherein said memory comprises:

a plurality of banks of write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein:

during a programming cycle for a selected memory cell in the array, the write circuit applies a first voltage to drive a current through the selected memory cell and change a threshold voltage of the selected memory cell; and

during a verify cycle for the selected memory cell, the write

circuit determines whether a threshold voltage of the selected memory cell has reached a target level representing a value being written into the selected memory cell;

a charge pump that generates the first voltage from a supply voltage and is coupled to the write circuits to supply the first voltage for the programming cycles; and

a timing circuit coupled to start programming cycles in the pipelines, wherein the timing circuit starts programming cycles for each bank at times that are different from when programming cycles start in the other banks.

17.(Amended) The system of Claim 16, wherein the plurality of banks comprises a first bank and a second bank, and the timing circuit starts programming cycles in the first bank when verify cycles start in the second bank.

18. A method for digital imaging, the method comprising:

converting an image into electrical signals;

storing said electrical signals as analog data; and

transmitting portions of said analog data for digital signal processing.

19. The method of Claim 18, further comprising pre-processing said electrical signals prior to said storing.

20. The method of Claim 18, wherein said analog data is stored at a rate greater than 10 Mbits/sec for more than 5 seconds and in a quantity greater than 50 Mbits.

21. The method of Claim 18, wherein said portions are transmitted only when said digital signal processing is available.

22. The method of Claim 18, wherein said converting and storing are performed in a digital still camera.

23. The method of Claim 18, wherein said storing comprises:

starting a first programming operation to program a first selected memory cell

in a first memory array, wherein the first programming operation includes connecting a charge pump to drive a current through the first selected memory cell and change a threshold voltage in the first memory cell; and

starting a second programming operation to program a second selected memory cell in a second memory array, wherein the second programming operation includes connecting the charge pump to drive a current through the second selected memory cell and change a threshold voltage in the second memory cell, wherein starting the second programming operation occurs after starting first programming operation but before the first programming operation is complete.

24.(New) A digital imaging system comprising:

an image sensor;

image processing and compression circuits; and

an analog/multi-level memory coupled between said image sensor and said image processing and compression circuits to receive and temporarily store analog data from said image sensor and transmit said analog data to said image processing and compression circuits, wherein said memory comprises:

a plurality of odd numbered write pipelines and a plurality of even numbered write pipelines, each write pipeline comprising:

an array of non-volatile memory cells; and

a write circuit coupled to the array, wherein when started on a programming operation for a selected memory cell in the array, the write circuit applies a first voltage to the selected memory cell to drive a current through the selected memory cell, wherein when an odd numbered pipeline and an even numbered pipeline are both performing programming operations, a selection circuit in the odd numbered pipeline selects the first voltage when a selection circuit in the even numbered pipeline selects a second voltage and a selection circuit in the odd numbered pipeline selects the second voltage when the selection circuit in the even numbered pipeline selects the first voltage.

25.(New) The system of Claim 1, wherein said stored analog data is externally accessible.

26.(New) The method of Claim 18, further comprising:

accessing said stored analog data in analog form prior to said transmitting.